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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/893,477	06/29/2001	Keiji Minetani	010781	5295

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EXAMINER
LEWIS, MONICA

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/893,477	Applicant(s) MINETANI, KEIJI	
	Examiner Monica Lewis	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This office action is in response to the application filed June 29, 2001.

Information Disclosure Statement

2. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered. Patent Application (Kokoku) Hei 6-71011 is disclosed in the specification however it is not listed on the Information Disclosure Statement (See Page 3 Lines 1-2).

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Appropriate correction is required.

Claim Objections

4. Claims 1 and 5 are objected to because of the following informalities: a) it appears that "dosed" should be "doped" (See Claim 1); and b) it appears that "sifts" should be "shifts" (See Claim 5). Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what is meant by the following: a) "energy band gap is made narrower inside than both ends by positioning a peak of a distribution of one constituent element into the inside and by continuously changing a ratio of the one constituent element in a thickness direction, and dosed with an impurity" (See Claim 1); and b) "a material that one constituent element is added" (See Claim 2). Claims 3-11 depend directly or indirectly from a rejected claim and are, therefore, also rejected under 35 U.S.C. 112, second paragraph for the reasons set above.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-5, 7, 8 and 11, as far as understood, are rejected under 35 U.S.C. 103(a) as obvious over Saito (U.S. Patent No. 5,773,853) in view of Applicant's Prior Art Drawings.

In regards to claim 1, Saito discloses the following:

a.) a substrate (21) formed of a first compound semiconductor (See Figure 4b);

b) a graded channel layer (23) formed on the substrate, and formed of a second compound semiconductor layer of which an energy band gap is made narrower inside than both ends by positioning a peak of a distribution of one constituent element into the inside and by continuously changing a ratio of the one constituent element in a thickness direction and dosed with an impurity (See Figure 4b);

c) a barrier layer (24) formed on the graded channel layer (See Figure 4b); and

d) a source electrode (S2)and a drain electrode (D2) formed both sides of the gate electrode (G2) to flow a current into the graded channel layer.

In regards to claim 1; Saito fails to disclose the following:

a) a gate electrode formed on the barrier layer to come into Schottky-contact with the barrier layer.

However, Applicant's Prior Art Drawings discloses a semiconductor device where the gate electrode is formed on the barrier layer (See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Saito to include a gate electrode formed on the barrier layer as disclosed in Applicant's Prior Art Drawings to aid in increasing the speed of the device.

In regards to claim 2, Saito fails to disclose the following:

a) the second compound semiconductor layer is composed of a material that one constituent element is added in the first compound semiconductor and the one constituent element has a function which makes the energy band gap of the second compound semiconductor layer narrower than that of the first compound semiconductor.

Although, Saito does not specifically disclose the limitations listed above. It would have been obvious that the second compound layer would have the characteristics stated above because both layers are made of $In_yGa_{1-y}As$.

In regards to claim 3, Saito fails to disclose the following:

a) a peak of the one constituent element in the graded channel layer is positioned at a center of a layer thickness of the graded channel layer, or positioned at a position that is deviated from the center.

Although, Saito does not specifically disclose the limitations listed above. It would have been obvious that the graded channel layer would have the characteristics stated above because both layers are made of $In_yGa_{1-y}As$.

In regards to claim 4, Saito fails to disclose the following:

a) a peak of carrier density in the graded channel layer is positioned at a center of a layer thickness of the graded channel layer, or deviates from the center.

Although, Saito does not specifically disclose the limitations listed above. It would have been obvious that the graded channel layer would have the characteristics stated above because both layers are made of $In_yGa_{1-y}As$.

In regards to claim 5, Saito fails to disclose the following:

a) a peak of carrier density in the graded channel layer sifts to the substrate side from a center of a layer thickness of the graded channel layer.

Although, Saito does not specifically disclose the limitations listed above. It would have been obvious that the graded channel layer would have the characteristics stated above because both layers are made of $In_yGa_{1-y}As$.

In regards to claim 7, Saito discloses the following:

a) a buffer layer (22) is formed between the substrate and the graded channel layer (See Figure 4b).

In regards to claim 8, Saito discloses the following:

a) the first compound semiconductor constituting the substrate is GaAs, and the second compound semiconductor layer constituting the graded channel layer is InGaAs, and the one constituent element contained in the second compound semiconductor layer is indium (See Figure 4b).

In regards to claim 11, Saito discloses the following:

a) second compound semiconductor layer (23) is consisted of a ternary or quaternary of group III-V semiconductor including at least one of gallium and indium as group III element and including at least one arsenic, phosphorus, and antimony as group V element (See Figure 4b).

9. Claim 6, as far as understood, is rejected under 35 U.S.C. 103(a) as obvious over Saito (U.S. Patent No. 5,773,853) in view of Applicant's Prior Art Drawings and Nakanishi (U.S. Patent No. 5,477,066).

In regards to claim 6, Saito fails to disclose the following:

a) contact layers are formed between the source electrode and the barrier layer and between the drain electrode and the barrier layer respectively.

However, Nakanishi discloses a semiconductor device which has a contact layer formed between the source and drain (See Figure 74 and Column 1 Lines 57-67). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Saito to include a contact layer as disclosed in Nakanishi to aid in increasing the speed of the device.

10. Claims 9 and 10, as far as understood, are rejected under 35 U.S.C. 103(a) as obvious over Saito (U.S. Patent No. 5,773,853) in view of Applicant's Prior Art Drawings and Kuroda et al. (U.S. Patent No. 5,837,565).

In regards to claim 9, Saito discloses the following:

a) first compound semiconductor constituting the substrate is GaAs (See Figure 4b).

In regards to claim 9, Saito fails to disclose the following:

b) second compound semiconductor layer constituting the graded channel layer is GaAsSb or InGaSb, and the one constituent element contained in the second compound semiconductor layer is indium or antimony.

However, Kuroda et al. ("Kuroda") discloses a semiconductor device which has a layer composed of GaAsSb (See Column 4 Lines 66-67 and Column 5 Lines 1-5). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Saito to include a layer composed of GaAsSb as disclosed in Kuroda to aid in increasing the speed of the device.

In regards to claim 10, Saito discloses the following:

a) the first compound semiconductor constituting the substrate is InP (11).

In regards to claim 10, Saito fails to disclose the following:

a) second compound semiconductor layer constituting the graded channel layer is InAsP or GaAsSb or InPSb, and one constituent element contained in the second compound semiconductor layer is indium or antimony.

However, Kuroda discloses a semiconductor device which has a layer composed of GaAsSb (See Column 4 Lines 66-67 and Column 5 Lines 1-5). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Saito to include a layer composed of GaAsSb as disclosed in Kuroda to aid in increasing the speed of the device.

Conclusion

11. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: a) Nakagawa (U.S. Patent No. 5,321,278) discloses a high electron mobility transistor; b) Ikalainen et al. (U.S. Patent No. 5,350,936) discloses a linear field effect transistor; c) Yagura et al. (U.S. Patent No. 5,719,415) discloses a hetero-junction bipolar transistor; d) Shimawaki (U.S. Patent No. 5,903,018) discloses a bipolar transistor including a compound semiconductor; e) Stanchina et al. (U.S. Patent No. 5,349,201) discloses a heterojunction bipolar transistor; f) Kuwata (U.S. Patent No. 5,206,527) discloses a field effect transistor; g) Kuwata (U.S. Patent No. 5,331,410) discloses a field effect transistor having a channel layer; and h) Unozawa (U.S. Patent No. 5,780,879) discloses a field effect transistor).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 703-308-4940. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and

after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML
March 12, 2002

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